Low–Dielectric Constant Insulators for Future Integrated Circuits and Packages

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Abstract

Future integrated circuits and packages will require extraordinary dielectric materials for interconnects to allow transistor advances to be translated into system-level advances. Exceedingly low-permittivity and low-loss materials are required at every level of the electronic system, from chip-level insulators to packages and printed wiring boards. In this review, the requirements and goals for future insulators are discussed followed by a summary of current state-of-the-art materials and technical approaches. Much work needs to be done for insulating materials and structures to meet future needs.

INTRODUCTION

The term dielectric was first used by William Whewell based on a request from Michael Faraday. A dielectric material is an electrical insulator that can be polarized when exposed to an external electric field. Most electronic systems (e.g., computers, radios, phones) are composed of integrated circuits (ICs) and electrically conductive pathways that power the ICs and transmit data. ICs (or chips) usually contain many layers of wiring so that the individual transistors can be formed into an electronic circuit, as shown in **Figure 1**. Some on-chip wires are short and connect nearby transistors (local wires), whereas others connect distant regions on the chip (global wires). ICs are packaged in a variety of ways so that the chip can be mechanically protected and electrically connected to other chips. The packaged chip is usually connected to a printed wiring board (PWB) containing many ICs and other components such as inductors, capacitors, and resistors. PWBs can electrically communicate through a backplane.

A variety of dielectric materials are used throughout the electrical system depending on the length of the electrical connection and nature of the surrounding materials. Most ICs are fabricated on a silicon substrate. IC packages are often composed of metal-polymer composite structures, such as epoxy reinforced with glass fibers (fiberglass), or ceramic substrates. **Figure 2** shows three possible configurations for interconnects. Coaxial cables are often used to connect backplanes. The stripline configuration is often used in PWBs, and the microstrip is similar to on-chip wiring.

BACKGROUND TO ELECTRICAL INSULATION

An electrical model for a uniform transmission line is shown in **Figure 3**. The electrical connection is shown as two parallel lines: signal and ground. The parameters, each per unit length of interconnect, are the resistance, R, and inductance, L, along the length of the line, and shunt capacitance, C, and conductance, G, both of which couple the signal and its return path. If the line is short or the rise time of the voltage pulse is long, the inductance can be ignored and the line can be represented simply by the series resistance and shunt capacitance (1). This occurs for local interconnects on-chip that connect transistors in close proximity. If the interconnect resistance and capacitance are treated as single, lumped values, then the voltage of the signal line rises as a single

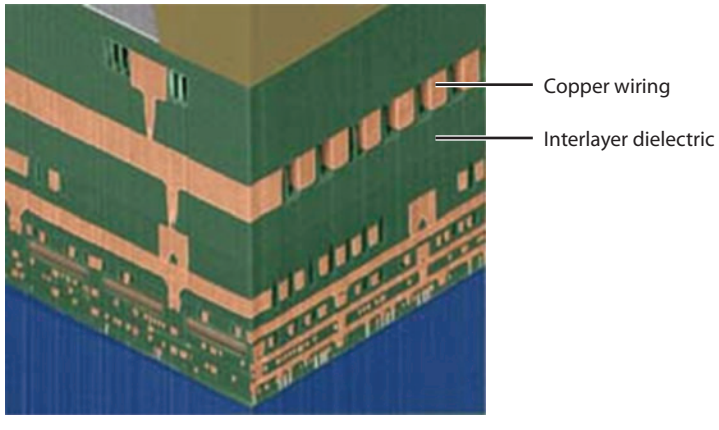


Figure 1

A cross-sectional view of an integrated circuit with many layers of copper wiring.

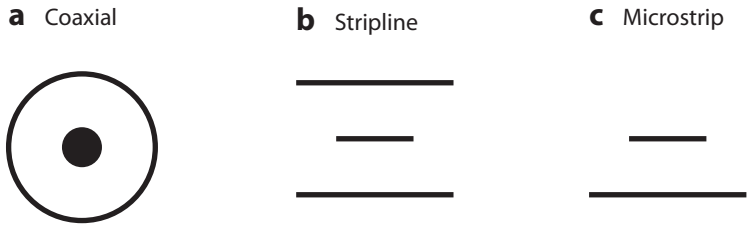


Figure 2

Three configurations of signal lines with return paths: (*a*) coaxial, (*b*) stripline, and (*c*) microstrip.

equipotential value in response to the application of an input voltage, as shown in Equation 1,

$$V\,(\text{out}) = 1 - \mathrm{e}^{\frac{t}{RC}}, \qquad 1.$$

where V(out) is the output voltage in response to an input voltage step from zero to value V, t is time, R is the resistance, and C is the capacitance. The product RC has units of time with 1 ohm F = 1 s. Thus, at one RC time constant, the output voltage rises to 63% of the input voltage. In this case, the capacitance of the dielectric material has equal importance to the resistance of the metal. The capacitance is proportional to the dielectric constant, as shown for a parallel plate capacitor in Equation 2,

$$C = \varepsilon_r \varepsilon_o A/d, \qquad 2.$$

where ε_0 is the permittivity of free space, ε_r is the relative dielectric constant, A is the capacitor area, and d is the dielectric thickness.

The relative dielectric constant is a complex number composed of the permittivity, ε_r', and loss, ε_r'', as shown in Equation 3 (1, 2),

$$\varepsilon_r' = \varepsilon_r' + \mathrm{i}\varepsilon_r'', \qquad 3.$$

where i is $\sqrt{-1}$. The permittivity is the stored energy in the medium, whereas the loss, ε_r'', represents the energy dissipated. Thus, for a local interconnect, Equation 1 establishes that the dielectric capacitance and metal resistance have equal weighting, and for high-quality, low-loss materials, the capacitance is dominated by the permittivity.

If the conductor line is long or the rise time of the applied voltage pulse is fast, the line inductance is important and the line must be considered a transmission line. An inductance resists changes in the current by generating a reverse electromotive force and thus introduces a limit to how fast a voltage pulse can propagate down the line. Unlike a short, RC-dominated line, a transmission line is not an equipotential structure, and the voltage travels down the line as a traveling wave. The simplest form for the electromagnetic wave propagation is a waveguide in the transverse electromagnetic mode in which the electric and magnetic modes in the waveguide have

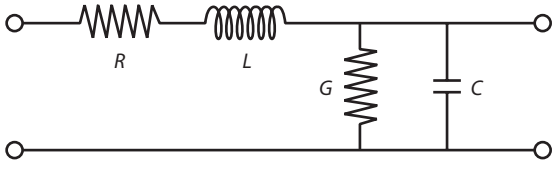


Figure 3

A transmission line model that shows resistance (R), conductance (G), inductance (L), and capacitance (C).

no component along the direction of propagation. Then, the electric and magnetic field vectors are perpendicular to the velocity vector and travel in the transversal planes.

There are two common types of transmission lines: lossless lines for which the resistance of the line is negligible, and lossy lines for which metal resistance is significant. Lossy lines often occur in long, global wires on-chip and in some thin-film packaging wires. Lossless lines occur in thicker wires on chip packages and in PWBs.

The propagation velocity of the voltage wave traveling down a lossless transmission line, v, is given by Equation 4:

$$v = \frac{1}{\sqrt{LC}}. \quad 4.$$

The characteristic impedance, Z_0, relates the voltage step to the current, I, traveling down a line using Ohm's law, as in Equation 5:

$$Z_0 = \frac{V}{I} = \frac{\sqrt{L}}{C}. \quad 5.$$

In addition to velocity limitations in a lossy line, there is also an attenuation of the electric field strength for a waveform traveling in the transmission line owing to resistance in the metal, skin effect losses in the metal, and dielectric loss. The ratio of the amplitude of the voltage waveform at some length, l, down a lossy transmission line, $V(x = l)$, to that of the voltage at the input of the transmission line, $V(x = 0)$, is given by Equation 6,

$$\frac{V(x = l)}{V(x = 0)} = \mathrm{e}^{-\gamma l}, \quad 6.$$

where γ is the attenuation constant, as given in Equation 7,

$$\gamma = \sqrt{(R + i\omega L)(G + i\omega C)} = \alpha + \mathrm{i}\beta, \quad 7.$$

where ω is the angular frequency (2π frequency), i is the square root of -1, β is the phase constant, and α is composed of conductor losses, α_c, (metal resistance and skin effect), and insulator loss, α_i (neper m^{-1}), as shown in Equation 8,

$$\alpha = \alpha_c + \alpha_i \quad 8.$$

The resistive part of the conductor loss is given by Equation 9, and the dielectric loss is given by Equation 10:

$$\alpha_c = \frac{\sqrt{\frac{\omega \mu_0 \varepsilon_r}{2\sigma\mu_r}}}{\eta_0 d}, \quad 9.$$

$$\alpha_i = \frac{\omega\sqrt{\mu_r \varepsilon_r}\tan\delta}{2c}, \quad 10.$$

where μ_0 is the permeability of free space, σ is the conductivity of the metal, μ_r is the relative permeability, η_0 is the characteristic impedance of free space (377 Ω), d is the separation distance between the signal line and its return path (dielectric thickness), tan δ is the loss tangent of the dielectric ($\varepsilon_r''/\varepsilon_r'$), and c is the speed of light in vacuo.

The typical voltage decay or attenuation of a signal carried by a transmission line on an epoxy-based PWB is shown in **Figure 4** (3). S_{21} is a ratio of the voltage at the exit (port 2) to the voltage of the injected signal at input (port 1), as measured in decibels (logarithmic unit). The nearly linear slope of the attenuation with frequency is evident from taking the log of Equation 6 and recognizing that the insulator loss, α_i, with its direct dependency on frequency, as seen in Equation 10, dominates.

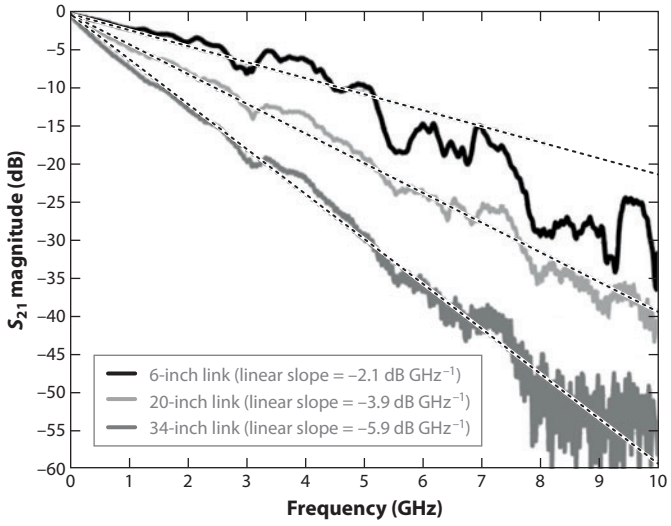


Figure 4

Voltage decay of the signal received at the output port compared with that injected at the input port, S_{21}, as measured in decibels, for three organic printed wiring boards of different lengths. Copyright © 2005 IEEE.

Thus, on one hand, the permittivity of the dielectric material often dominates the dielectric performance and time constant for short, *RC* lines. On the other hand, the dielectric loss (through the loss tangent) dominates the attenuation of transmission lines at high frequency because the attenuation is directly proportional to ω, whereas the conductor loss is proportional to $\omega^{1/2}$.

MATERIALS REQUIREMENTS

The permittivity and loss are a function of frequency. There are several frequency-dependent contributions to the dielectric constant, as given by the Debye equation, Equation 11,

$$\frac{\varepsilon_r - 1}{\varepsilon_r + 2} = \frac{N}{(3\varepsilon_0)}\left(\alpha_e + \alpha_d + \frac{\mu^2}{3kT}\right), \qquad 11.$$

where N is the number density of dipoles in the insulator, α_e is the electronic polarization, α_d is the distortion polarization, μ is the orientation polarizability, k is the Boltzmann constant, and T is the absolute temperature. The term $\frac{\mu^2}{3kT}$ is often referred to as the orientation polarization.

The polarizations (electronic, distortion, and orientation) each have a different origin and frequency dependency, as shown in **Figure 5** (2). Electronic polarization arises from a distortion of the electron cloud around the nucleus of the atom and follows changes in the electric field virtually instantaneously. It is the only contribution to the dielectric constant at high frequencies (e.g., $>4.74 \times 10^{14}$ Hz or 633-nm wavelength) where the dielectric constant approaches the square of the index of refraction. Distortion polarization, which is sometimes called atomic polarization, reflects the bending and stretching of the molecule as the dipole is changed under the influence of an electric field. Its effect occurs at frequencies greater than 10^{11} to 10^{14} Hz, which is within the infrared part of the spectrum. Both electronic and distortion polarization possess restorative forces when the electric field is changed; these forces give rise to a resonance at a particular frequency. Orientation polarization occurs only at lower frequencies because it requires the movement of ions or molecules, such as the rotation of permanent dipoles or displacement of ions. There is

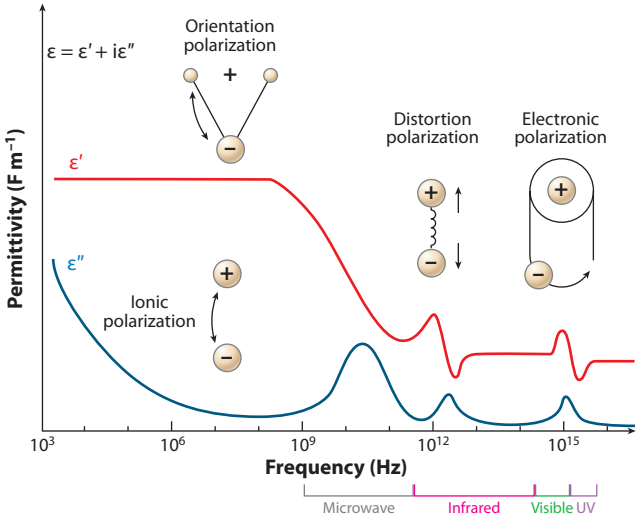


Figure 5

Permittivity and loss of a dielectric material as a function of frequency.

no restorative force and resulting resonance for orientation polarization because the dipole itself (distance between charges) remains unchanged. At the frequencies of interest in modern electronic devices (e.g., gigahertz), orientation polarization does not contribute because the time constant is too slow.

Many types of insulators have been developed for ICs and packages, as reviewed in previous publications (4–7). There are two general strategies for lowering the dielectric constant of insulators: (*a*) to choose materials and chemical moieties that have inherently low polarizability, and (*b*) to lower the density of dipoles within the material. Equation 11 clearly shows that lowering the number of dipoles, *N*, within the insulator results in a lower dielectric constant given that the dipoles are of the same type. This strategy has led to the creation of porous materials in which the creation of free volume in the insulators lowers the density.

Table 1 shows the electronic polarizability of different chemical bonds (8, 9). The polarizability of sigma bonds is lower than that of pi bonds, which makes saturated hydrocarbons the choice for organic insulators. The high electronegativity of fluorine causes its nucleus to tightly hold its electrons, which gives the C–F bond lower polarizability than the C–H bond. Thus, fluorination of

Table 1 Electronic polarizability of specific chemical bonds

Bond	Polarizability, A^3	Bond Strength, kcal mol^{-1}
C–C	0.531	83
C–F	0.555	116
C–O	0.584	84
C–H	0.652	99
O–H	0.706	102
C=O	1.020	176
C=C	1.643	146
C≡C	2.036	200
C≡N	2.239	213

Table 2 2009 International Technology Roadmap for Semiconductors values for on-chip interconnect for high-performance microprocessors

Production year	2010	2012	2014	2016	2018	2020	2022	2024
Technology node[a] (nm)	45	32	24	19	15	12	9.5	7.5
Bulk dielectric constant, minimum	2.3	2.3	2.1	1.9[b]	1.9[b]	1.7[b]	1.5[b]	1.4[b]
Effective dielectric constant, minimum	2.6	2.6	2.4	2.1[b]	2.1[b]	2.0[b]	1.7[b]	1.7[b]
Capacitance per length for global wires (pF cm^{-1})	1.8	1.8	1.7	1.5	1.5	1.4	1.2	1.2
RC delay for 1-mm Cu wire with no scattering (ps)	1.13	2.23	2.69	5.23	8.34	12.53	19.55	24.74

[a]Technology node is also referred to as metal 1 microprocessor half pitch.
[b]Values are identified as having no known solutions.
R, resistance; *C*, capacitance.

hydrocarbons is an important approach to lowering the dielectric constant. The mobility of the pi electrons in double and triple bonds makes them more easily polarized than sigma bonds. However, the bond strength of pi bonds is highly desired for mechanical properties. The dielectric constant is often dominated by distortion polarization effects owing to polar moieties within insulators such as hydroxyl and carbonyl groups. Absorbed water is especially important because it has a very high relative dielectric constant, 78, can adsorb and desorb to cause a change in the dielectric constant under different ambient conditions, and is an essential component of metal corrosion.

The International Technology Roadmap for Semiconductors (ITRS) (10) summarizes the future dielectric needs for ICs and chip packages. **Table 2** shows select values for on-chip, microprocessor (MPU) dielectrics. The bulk dielectric constant for local interconnects is targeted to decrease from 2.3 in 2010 to 1.4 in 2024. There is no known solution to obtaining values at or below 2.1. This yields an effective dielectric constant of 2.6 in 2010 and 1.7 in 2024. The effective dielectric constant is higher than the bulk value owing to fringing fields in the surrounding material. The decrease in the dielectric constant will result in a decrease in the capacitance from 1.8 pF cm^{-1} in 2010 to 1.2 pF cm^{-1} in 2024. Even with this decrease in capacitance, the *RC* constant for a 1-mm-long wire is still expected to rise from 1.13 ps to 24.74 ps in 2024. This reflects the increase in wire resistance owing to shrinking dimensions and smaller spacing between wires.

Low–dielectric constant materials (also called low-*k*) are also needed in electronic packages and substrates. **Table 3** shows select ITRS values for high-performance chip substrates. Of particular interest is the increase in on-chip frequency from 5.88 GHz in 2010 to 15.51 GHz in 2024 as well as the increase in chip-to-substrate data rate per pin from 10 Gbit s^{-1} in 2010 to 75 Gbit s^{-1} in 2024. This extraordinary chip-to-substrate data rate per pin reflects the need for greater aggregate bandwidth between MPUs and other components, especially memory chips, and the constraint on the number of input/output pins. Epoxy-based organic substrates will still be used for many lower-performance chip packages; however, the ITRS identifies a change in high-performance substrates to silicon-based structures in 2015. The dielectric constant and loss are anticipated to decrease in future years to values similar to on-chip dielectrics. However, the dielectric loss is also specified for off-chip applications because of the long wire length and exceedingly high data rate. The critical need for lower permittivity and lower loss dielectrics is evident in **Figure 4**, as the voltage attenuation becomes more severe in a transmission line at higher frequency for a given line length. A minimum value of signal strength at the output is required so that the bit error rate is acceptable. A typical acceptable attenuation value is −20 dB. If this is applied to **Figure 4**, then

Table 3 2009 International Technology Roadmap for Semiconductors values for high-performance microprocessor packaging

Production year	2010	2012	2014	2016	2018	2020	2022	2024
On-chip frequency (GHz)	5.88	6.82	7.91	9.18	10.65	12.36	14.34	15.51
Chip-to-board data rate (Gbit s^{-1})	10	14	24	35	45[a]	55[a]	65[a]	75[a]
Typical buildup material	Polyimide	Polyimide	Polyimide	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2
Buildup material T_g (°C)	300	300	300	700	700	700	700	700
Buildup material CTE (in-plane)	16	16	16	3	3	3	3	3
Buildup material CTE (through-plane)	20	20	20	16	161	16	16	16
Dielectric constant, 1 GHz	3.3	3.3	3.3	2.0	2.0	1.8	1.8	1.8
Dielectric loss, 1 GHz	0.038	0.038	0.038	0.003	0.003	0.001	0.001	0.001
Young's modulus (GPa)	5	5	5	10	10	10	10	10

[a]Values are identified as having no known solutions.
Abbreviation: CTE, coefficient of thermal expansion.

the 6″ transmission line would be limited to less than 8-GHz performance, far short of the future ITRS targets.

The output signal strength could be improved by increasing the voltage of the input pulse. This would keep the output voltage above the noise level over longer traces at the same frequency or allow the same transmission line to be used at a higher frequency (see **Figure 4**). However, this approach is not generally acceptable owing to the excess energy required to transmit data. ICs, especially MPUs, are power limited. The power of high-performance MPUs is capped at 198 W through the end of the ITRS because of the difficulty in delivering dc power to the chip, the difficulty in removing heat at higher power, and the cost of electricity in operating electronic devices. Interconnects already consume a majority of the energy used by high-performance devices. The energy to charge a capacitor, such as the capacitance in **Figure 3**, is $CV^2/2$, where V is the voltage. Thus, the power consumed by a wire operating at a given frequency, f, is given by Equation 12:

$$Power = fCV^2. \quad 12.$$

Thus, increasing the voltage to allow higher frequency operation of a wire is not an option. In fact, signaling techniques that allow operation of wires at low voltages, in particular voltages lower than those of the transistors (sometimes called low-swing interconnect), are of great interest as a mechanism to lower interconnect power.

The two most effective approaches to achieving a low dielectric constant are (*a*) lowering the polarizability of the material and (*b*) decreasing the density (i.e., number of atoms present per unit volume). The issue of polarizability has already been discussed. **Table 4** shows the dielectric constant and square of the index of refraction for several dielectric materials (6). The square of the index of refraction represents the electronic polarization, and the difference between it and the dielectric constant in the MHz range reflects the distortion polarization. The effect of the permanent dipole in the Si–O bond on the distortion polarization, as well as the benefits of C–F bonds and C–C bonds in organic compounds, can be seen. A detailed description of the materials in **Table 4** is given in the next section.

Thus, to obtain lower effective dielectric constants, the number density of atoms in the insulator, N in Equation 11, must be lowered. To achieve this, porous materials incorporate a gas, usually

Table 4 Dielectric constant and square of index of refraction for several dielectric materials

Dielectric material	Relative dielectric constant	Square of index of refraction
Polytetrafluoroethylene (PTFE)	1.92	1.80
Polyimide, BPDA-PDA	3.12	2.61
Polyimide, PMDA-TFMOB-FDA-PDA	2.65	2.30
Polyarylene ether	3.00	2.79
FLARE®	2.8	2.8
Cyclotene®	2.65	2.41
SiLK	2.65	2.64
MSQ/HSQ	2.52	1.89
Parylene-F	2.18	2.04
Parylene-N	2.58	2.47
SiO_2	4.0	2.16

Abbreviations: BPDA-PDA, biphenyl dianhydride-*p*-phenylene diamine; PMDA-TFMOB-FDA-PDA, pyromellitic acid dianhydride bis(trifluoromethoxy)benzidine (4,4′-hexafluoroisopropylidene) biphenyl dianhydride *p*-phenylene diamine; MSQ/HSQ, methylsilsesquioxane/hydrogen silsesquioxane.

air, in the solid network. It is important that the pores have closed walls (be entirely surrounded by the network material) and be small in size when compared with the thickness of the insulating layer so that contiguous channels or pathways between the two metal plates of the capacitor (the wire and its return path) are not formed. In particular, a contiguous pathway between two copper wires could form an ionic pathway for corrosion. Also, the pore walls should be hydrophobic so as not to absorb water. If the pores are small and spherical in shape, the effective dielectric constant of the matrix, ε_r, is given by Equation 13,

$$\frac{\varepsilon_r - 1}{\varepsilon_r + 2} = P\frac{\varepsilon_1 - 1}{\varepsilon_1 + 2} + \frac{(1-P)(\varepsilon_2 - 1)}{\varepsilon_2 + 2}, \qquad 13.$$

where ε_1 is the relative dielectric constant of the material inside the pores (essentially 1 if it is air), ε_2 is the relative dielectric constant of the network material encapsulating the pores, and P is the fractional porosity. For example, if silicon dioxide ($\varepsilon_r = 4$) were made 50% porous with air inside the pores, the effective dielectric constant would be approximately 2.1. Nonspherical pores can have higher or lower effective dielectric constants depending on the orientation of the pores. Orientation in the direction of the electric field, for example, will lower the effective dielectric constant even further.

Although it appears that many materials can be used to achieve relative dielectric constants lower than 3, and the incorporation of porosity can be used to decrease the dielectric constant below 2, the integration of low-*k* materials into ICs and electronic packages has been exceedingly difficult and is far behind schedule. The difficulties arise from the mechanical and chemical properties, cost, and reproducibility (integration) requirements for the insulators.

In addition to the permittivity and loss criteria stated above, dielectric materials must withstand the elevated processing temperatures, oxidative chemical environment, and high mechanical stresses that occur on-chip and in packages. Resistance to thermal degradation is critical because decomposition generally leads to poor electrical properties, and the molecular products can cause copper corrosion. As shown in **Table 4**, less stable sigma bonds generally must be chosen over more stable pi bonds.

Thermal stability is required because the on-chip metal is annealed to increase its conductivity. Furthermore, subsequent dielectric layers need to be heated during deposition or curing, and

assembly of the chip onto the substrate usually requires a thermal treatment for solder reflow or dielectric curing. Aluminum wiring is typically annealed at approximately 450°C. However, copper can be annealed at lower temperatures, <350°C, which allows more dielectric materials to be considered. The need for low-*k* materials originated when aluminum was still used on leading-edge ICs, but copper has replaced aluminum as the metal of choice owing to its higher electrical conductivity. Low-*k* inorganic insulators can have greater thermal stability than organic ones, although Si–H and Si–C bonds can be susceptible to decomposition in oxygen-rich environments (11, 12).

Mechanical strength and fracture toughness are critically important for dielectric materials. Thermally induced stresses are unavoidable because the two basic building materials for most electronic systems are (*a*) low–coefficient of thermal expansion (CTE) silicon ICs (CTE of 3 ppm $°C^{-1}$) and (*b*) copper wiring on chip substrates and PWBs (the CTE of copper is 16.5 ppm $°C^{-1}$). The temperatures used to fabricate the on-chip wires (approximately 350 to 450°C) and to assemble the chip onto the substrate (>200°C for epoxy molding or solder reflow), as well as the repeated temperature cycling when the component is used in-service, all create stresses owing to the CTE mismatch between silicon and the copper-dominated substrate and package. The dielectrics must be able to withstand the stresses without initiating or propagating cracks or delaminating from surfaces.

The mechanical stresses and expansion of the dielectric can also cause failures in multilayer, composite structures, such as buckling of overlayers (13). Processes such as chemical-mechanical polishing of wafers can damage films that lack adequate mechanical strength. The elastic modulus of the dielectric is often used as an indication of mechanical stability for low-*k* materials; this is often an order of magnitude lower than traditional insulators, especially for organic low-*k* materials (14).

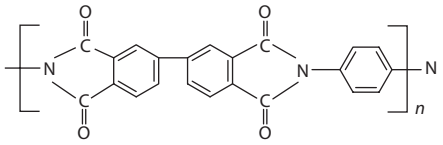
Finally, the cost of integrating a new material into existing products, including the cost of additional process steps for low-*k* solutions, is a major barrier to implementation. ICs are highly cost competitive. The lowest cost, highest yield, fastest to market product is most often chosen. Especially when radically new materials are considered, the complexity of integrating low-*k* materials, such as replacing an inorganic glass with an organic polymer, has led to major delays in the use of new materials. The unknown in-service reliability of new materials exacerbates the overall low-*k* situation.

CANDIDATE LOW-*k* MATERIALS

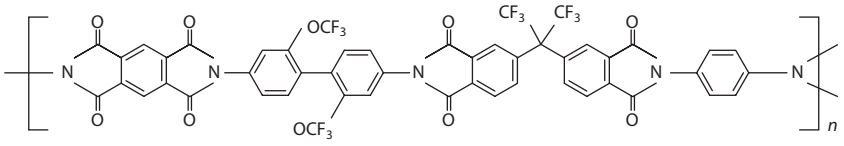
ICs have evolved using mainly silicon dioxide as the on-chip dielectric material. Plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 from silicon-containing precursors, such as tetraethoxysilane, is the primary route to depositing insulators on-chip (15). Organic chip substrates and PWBs use primarily epoxy-based materials. In the next section, many of the most important materials explored for on-chip and off-chip low-*k* solutions are reviewed. Finally, the most promising approaches to ultra-low-*k* insulators are discussed.

Organic Materials

Polytetrafluoroethylene (PTFE) has the lowest dielectric constant of all the fully densified materials considered. It takes advantage of the low polarizability of the C–F and C–C bonds in the perfluorinated structure (16). However, it suffers from many drawbacks including low elastic modulus (0.5 GPa), high CTE (>100 ppm $°C^{-1}$), and poor adhesion to surfaces. The incorporation of cyclic structures into the PTFE backbone results in amorphous, soluble compounds that can



BPDA–PDA polyimide



PMDA TFMOB 6FDA PDA

PMDA–TFMOB–FDA–PDA polyimide

Figure 6

Chemical structures of two polyimides: biphenyl dianhydride-*p*-phenylene diamine (BPDA PDA) and pyromellitic acid dianhydride bis(trifluoromethoxy)benzidine (4,4′-hexafluoroisopropylidene) biphenyl dianhydride *p*-phenylene diamine (PMDA-TFMOB-6FDA-PDA).

be spin-coated, such as Teflon AF® (17). Also, the high cost of manufacturing perfluorinated polymers is another barrier to high-volume use.

Many polymer dielectrics containing aryl and imide rings have been created; these are generally classified as polyimides. The original motivation for development of polyimide dielectrics was as a low-cost alternative to on-chip silicon dioxide (18). Polyimides are typically characterized by high glass transition temperature (T_g), high modulus, and low dielectric constant as compared with silicon dioxide. Rigid, aromatic polyimides are nearly insoluble in organic solvents. Polyimide films can be formed by solvent casting the polymer when in the precursor form of polyamic acid, followed by thermal curing to yield the polyimide (19–27). The aryl and imide rings make the polymer backbone of polyimides more rigid than aliphatic polymers. This increases the elastic modulus to >8 GPa and T_g to 350 to 400°C (19).

Polyimides are synthesized from the reaction of a diamine and dianhydride. The structure of two polyimides is shown in **Figure 6**. The introduction of partial fluorination, as in the case of pyromellitic acid dianhydride bis(trifluoromethoxy)benzidine (4,4′-hexafluoroisopropylidene) biphenyl dianhydride *p*-phenylene diamine (PMDA-TFMOB-6FDA-PDA), lowers the dielectric constant, as shown in **Table 4**, as well as the moisture uptake. The rigidity of the polymer backbone leads to orientation of the polymer strands during spin coating, which gives some polyimides direction-dependent (often called anisotropic) properties. The in-plane CTE of some polyimides can be <10 ppm $°C^{-1}$, whereas the through-plane CTE can be more than ten times greater (21). The anisotropy affects all properties including the dielectric constant. Unfortunately, the in-plane dielectric constant, which is the more important value, is higher than the through-plane value.

Polyimides have found many niche uses in electronic devices, especially as the final passivation layer on ICs and the interlayer dielectric on ceramic and silicon electronic packages. However, the curing of polyamic acid and formation of the imide is not compatible with epoxy-based printed circuit board temperatures, as epoxy boards cannot be heated above approximately 250°C without degradation.

Polyarylethers were created in an attempt to balance dielectric and mechanical properties. Their aryl rings make polyarylethers more rigid than PTFE but more flexible and isotropic than

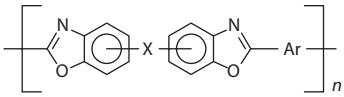


Figure 7

Chemical structure of polybenzoxazole.

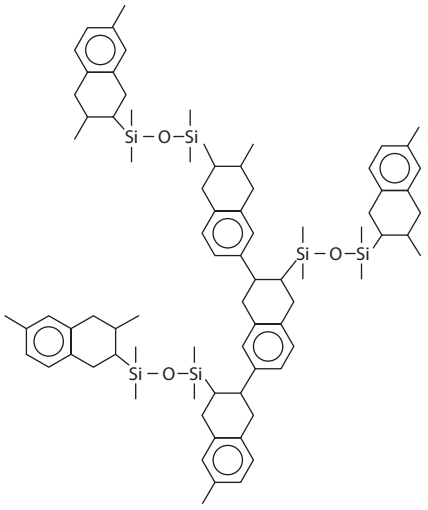
polyimides. Furthermore, the absence of the polar carbonyl groups found in polyimides lowers the dielectric constant and water absorption of polyarylethers. For example, one fluorinated polyarylether, marketed under the trade name FLARE, has a relative dielectric constant of 2.4, compared with 2.8 for its hydrocarbon form (22, 28–31). The thermal stability of polyarylethers is excellent, with only 2% weight loss when held at 425°C for 8 h; however, the low T_g (approximately 275°C) for the noncross-linked material is a concern (6).

Polybenzoxazoles are a family of high-temperature polymers similar in structure to polyimides (**Figure 7**). The use of flexible groups at the X and Ar positions in **Figure 7**, such as to form bis(*ortho*-amino-phenol), gives the films excellent solubility, T_g, and processability (32). Larger functional groups can also be used to further increase the solubility, but this comes at the expense of lower T_g. The processing is similar to that of polyimides; a soluble precursor, such as polyhydroxyamide, is solvent cast followed by curing to form the final polybenzoxazole. As in the case of polyimides, the final product is insoluble in the original casting solvent so that multilayered structures can be made. Fluorination of the phenyl groups and addition of trifluoromethyl groups has been used to lower the dielectric constant of polybenzoxazoles (33–35).

Polynorbornene is a polymer composed of a seven-carbon, saturated, dicyclic hydrocarbon backbone (36, 37). The stiff nature of the backbone and pure hydrocarbon content gives polynorbornene a high T_g (>350°C) as well as low dielectric constant (approximately 2.2 for the unfunctionalized polymer), residual stress, and water uptake. When polymerized in the atactic form, the polymer is soluble in a variety of solvents and can be spin cast (38). This combination of properties makes polynorbornene an interesting candidate for on-chip stress buffer applications (i.e., final passivation layer) as well as for an interlayer dielectric for electronic packages. Functional groups have been grafted onto the polynorbornene backbone to give it adequate adhesion and cross-linking (37). In particular, alkoxysilyl groups have been used to enhance adhesion to metal oxide surfaces, epoxy groups have been used to provide cross-linking, and alkyl groups have been used to improve the fracture toughness. Polynorbornene is also optically transparent to visible light, which makes it applicable to chip-based optical sensors and cameras.

Bis(benzocyclobutene) (BCB), which was commercialized under the trade name Cyclotene by Dow Chemical, is shown in **Figure 8** (39). The cyclobutene end groups can undergo a Diels-Alder cycloaddition reaction to give a thermoset product. The spin-cast solution contains partially reacted (so called B-staged) BCB monomers. Full curing of the oligomers can be accomplished at 250°C (40). Because the cyclobutene ring opening reaction does not require other reactants and does not evolve reaction products such as water or alcohol, as in the case of polyimides, polybenzoxazole, and epoxies, the films can be rapidly cured at higher temperature. The relative dielectric constant of cured films is 2.6 to 2.7. The films are thermally stable up to 375°C and have low water uptake, approximately 0.2% (41–43). The T_g is high, 350°C, but the CTE is also high at 52 ppm $°C^{-1}$. In addition, the films exhibit high residual stress, which helps produce planar surfaces when coated on substrates with existing topography but also adds to the mechanical problems of the final device (41, 43, 44).

Many of the polymer dielectrics discussed above do not fully meet on-chip thermal stability requirements because of the requirements of metal annealing. In an effort to address on-chip



Bis(benzocyclobutene) (BCB)

Figure 8

Chemical structure of cured bis(benzocyclobutene) (BCB).

interlayer dielectric needs, Dow commercialized a high-temperature polymer under the trade name SiLK (**Figure 9**) (45). Similar to BCB, SiLK is a partially cured mixture of oligomers that can be spin cast from a solvent followed by full curing at approximately 450°C for 6 min (after lower temperature soaks) (46). SiLK has a relative dielectric constant of 2.6–2.7 and a decomposition temperature of >500°C. Significant efforts were put into integrating SiLK as a low-*k*, on-chip interlayer dielectric, given its excellent dielectric constant and thermal stability (46). However, mechanical stresses owing to its high CTE (54 ppm $°C^{-1}$) caused layer-to-layer metal fracture on-chip, particularly at metal vias where one layer of copper wiring is connected to the next layer of copper wiring through a metal via connection.

Poly(1,4-xylene)s, commonly called Parylenes, were developed as electrical insulators owing to their ability to provide conformal coatings (47, 48). Parylenes are deposited by chemical vapor deposition (CVD) from a gaseous precursor such as *para*-cyclophane. Heating the precursor gas to >650°C causes the *para*-cyclophane to decompose into two 1,4-xylylidenes, which then deposit onto the cool target substrate and further react to form a linear polymer with excellent stability (47, 48). In addition to the hydrocarbon form (Parylene-N), there are also halogenated forms including Parylene-C (monochloro), Parylene-D (dichloro), and Parylene-F (fluorinated). Parylene-N has

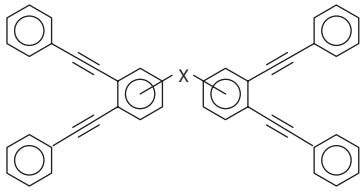


Figure 9

Chemical structure of SiLK.

a low relative dielectric constant (2.6) and elastic modulus (2.4 GPa) as well as a high CTE (42–69 ppm $°C^{-1}$) (48, 49). Use of Parylene has been inhibited owing to high weight loss at 400°C (up to 10% h^{-1}), and the potential cost and complexity of running an organic CVD reactor (47). Parylene-F, which replaces the aliphatic hydrogens with fluorine, was introduced to improve the thermal stability and dielectric constant compared to Parylene-N. The relative dielectric constant was improved to 2.2 from 2.4, and the thermal stability was improved to 0.8% h^{-1} weight loss at 450°C (42, 50, 51).

Inorganic Materials

The use of SiO_2 (which has a relative dielectric constant of 4.0 to 4.2) as the on-chip insulator of choice originates with the selection of silicon itself as the semiconductor of choice for ICs. Silicon was chosen over germanium and compound semiconductors owing to its formation of a stable, insoluble, chemically inert oxide (i.e., SiO_2). SiO_2 is nearly CTE matched to silicon (CTE of 0.5 ppm $°C^{-1}$ for SiO_2 versus 3 ppm $°C^{-1}$ for silicon) and grown by oxidation of silicon or deposited via other methods such as PECVD.

Low-*k* SiO_2 was first produced by introducing fluorine into SiO_2 to yield fluorosilicate glass (FSG). FSG also can be produced by (*a*) liquid phase deposition from a saturated solution of fluorosilicic acid (52, 53), (*b*) gas phase deposition using fluorotrialkoxysilanes (54–56), or (*c*) plasma-assisted deposition using tetraethoxy silane and a fluorine source such as CF_4, C_2F_6, or SiF_4 (57). Plasma deposition is by far the most used process.

Lowering the relative dielectric constant of fully densified SiO_2 below 3.5 requires introduction of silicon-carbon bonds so as to reduce the average bond polarity. Amorphous materials described as SiCOH (the generic set of elements included in the film) have become important partly because of their similarity to SiO_2. The PECVD deposition of SiCOH is similar to that of SiO_2 and has greatly eased problems with integration into the manufacture of silicon ICs. SiCOH was successfully implemented in IBM MPUs at the 90-nm node ($\varepsilon_r = 3.0$) and 65-nm node ($\varepsilon_r = 2.7$) (58, 59). A wide variety of organosilane precursors has been used to produce low-*k* SiCOH (4). In general, compounds with less than one oxygen atom per silicon in their structure (e.g., trimethylsilane, tetramethylsilane, dimethylphenylsilane, diphenylsilane, diphenylmethylsilane, and hexamethyldisiloxane), codeposited with an oxidant (e.g., N_2O or O_2), are preferred (60, 61). Radio frequency (13.56 MHz) plasma-assisted deposition of tetramethylsilane with N_2O or O_2 produced the first thermally stable SiCOH material with a dielectric constant of 3.1 (60–63). It is important to create network-forming Si–O–Si bonds in the SiCOH film. Reacting silicon compounds containing very few oxygen with N_2O or O_2 can lead to the oxidation of C–H bonds, which makes it difficult to control the number of terminal methyl bonds (64–66). This led to the use of cyclic siloxanes that have a greater number of Si–O bonds in the reactant than the previously mentioned compounds. Plasma-deposited SiCOH is commercially an important material for achieving low–dielectric constant insulators on-chip today.

Another family of plasma-assisted amorphous compounds is the amorphous or diamond-like carbon materials (64, 65). Amorphous carbon can be obtained by plasma-assisted deposition of films using fluorocarbon gases (66, 67). These materials have less acceptable thermal and mechanical properties compared with silica-based materials and are not widely used as dielectrics.

Solvent cast, spin-on silica compounds have also been used to lower the density and dielectric constant of SiO_2. Silsesquioxane (SQ)-based materials are inorganic-organic polymers with the general formula $(R–SiO_{1.5})_n$. That is, one of the four Si–O bonds in SiO_2 is replaced by a different functionality, R. Two common forms are obtained by replacing the Si–O bond with hydrogen atom to yield hydrogen silsesquioxane (HSQ) and by replacing the bond with a methyl group to

yield methyl silsesquioxane (MSQ). The density of HSQ is as low as 1.6 g cm^{-3}, compared with 2.2 to 2.4 g cm^{-3} for SiO_2. Generally, MSQ has a lower dielectric constant than HSQ owing to the low polarizability of the Si–CH_3 bond.

SQ can exist in a ladder or cage configuration. The cage structure has eight silicon atoms at the vertices of a cube. Although the silica structure is stable at high temperature, SQ compounds in the cage structure are highly sensitive to thermally activated redistribution processes and to oxidation at temperatures greater than 350°C in the presence of even low levels (ppm) of oxygen (68–70). Another issue with SQ compounds is the absorption of moisture (71, 72). Physisorbed moisture can be desorbed below 200°C, and weakly bound moisture can be desorbed at 400°C. More tightly bound moisture results when the R group is lost in a thermal or plasma process, which results in the formation of Si–OH (73). The typical moisture content is 2.2% for HSQ and 1.3% for MSQ.

CANDIDATE ULTRA LOW-*k* MATERIALS

The ITRS indicates that the on-chip and off-chip relative dielectric constant will decrease to the 2.0 level in 2016. This will require a high degree of porosity for any dielectric or the incorporation of air gaps on-chip as well as in packages and boards. Porous materials are being introduced at the 45-nm and 32-nm complementary metal oxide semiconductor nodes to achieve dielectric constants of 2.2 to 2.4. There are three general approaches to creating porosity. First, the reactants can be specifically chosen so as to create a low-density network during deposition. Second, the deposited film can be chemically treated after deposition to modify the network to lower the density and/or polarizability, such as by replacement of a bulky group with a small group. Third, a second phase, which can be removed after deposition, can be incorporated into the network by subsequent processing. The second labile phase is sometimes referred to as a porogen or sacrificial placeholder.

Porous Dielectrics

All three strategies have been used to form porous SiCOH. Following the first approach, mixtures containing methylsilane, dimethylsilane, or trimethylsilane with oxygen and argon were plasma deposited to produce a porous matrix with a dielectric constant of 2.4 to 2.6 after annealing at 550°C (74). Trimethylsilane gave the lowest dielectric constant. In another study, ring-opening monomers with unsaturated hydrocarbons were used to deposit films from a helium plasma (75). The ring structures survived the deposition process and resulted in relative dielectric constant values of less than 2.5. Using the second approach, postdeposition processes were used to create pores in SiCOH films. A dense SiCOH film containing Si–CH_3 groups was plasma treated at 400°C followed by exposure to a hydrogen plasma to modify the organosilane network (76). The plasma treatment converted the Si–CH_3 groups to Si–H without network collapse, thus leaving excess free volume in the film. This resulted in 1.2- to 3-nm pores and a relative dielectric constant of 2.4. In another case, hydrofluoric acid was used to partially etch a PECVD film deposited at 400°C using trimethylsilane and N_2O as the reactants (77). The pore size was controlled by the HF treatment, and the dielectric constant of the product was 2.7. In the third approach, a porogen is attached to the network. The porogen can be a part of the starting material or a second compound added to the reaction mixture. In one study, organic compounds were added to a PECVD SiCOH film. For example, vinyltrimethylsilane (versus just trimethylsilane) was included, which resulted in a film with a dielectric constant of 2.0 (78). A wide variety of organic porogens has been investigated including 1-hexene, bicyclohexadiene, norbornene, α-terpinene, cyclohexene oxide, cyclopentene

oxide, and butadiene monoxide. The sacrificial component can be removed by a thermal or UV treatment (79). This final approach using a sacrificial material is generally preferred because the amount of porosity and conditions for creating the pores can be controlled more easily.

Most of the spin-on dielectrics discussed above have been made porous, usually by incorporation of a porogen. For example, polyimides were made porous by incorporation of a sacrificial second, thermally labile material or by using polyimide nanoparticles (80–85). With these methods the dielectric constant can be lowered to approximately 2.0, but achieving uniform, small pores remains a challenge.

Porous SiLK was achieved by thermally grafting poly(ethylene glycol) methacrylate onto ozone-treated SiLK (86). This lowered the relative dielectric constant from 2.6 to 2.2, the target value. However, the pore size was too large. In another experiment, cross-linked polystyrene nanoparticles were used to create 5- to 8-nm pores (87). Porous SiLK was evaluated as an on-chip, low-*k* interlayer dielectric, but it was not used in favor of other plasma-deposited materials such as SiCOH (88, 89).

A variety of other spin-on dielectrics, including HSQ and MSQ, have been made porous by use of porogens (90–95). The approach generally involves mixing a thermosetting polymer in a solvent with a second, soluble component, the porogen. Several requirements must be met. First, both porogen and network-forming compound need to be soluble and compatible with each other in the solvent, or phase segregation will occur. Second, the matrix and porogen also must form a well-mixed colloidal dispersion when the solvent is removed. Third, the thermosetting matrix has to stiffen prior to removal of the porogen so that network collapse does not occur. When a porogen is simply mixed with the network-forming precursor, the network formation conditions must be carefully matched to the strengthening of the network. If adequate concentration of porogen is not used, the pore density may be too small. If excessive phase segregation occurs before network strengthening, the pores may be too large. Thus, approaches that bond the porogen to the network-forming compound seem inherently more likely to succeed, especially when high porosity is desired.

Many pore-forming compounds have been used to make well-formed, closed wall pores in spin-on glasses. For example, polycaprolactone has a star shape, indicating that spherical pores will be formed. Polycaprolactones can be synthesized in a range of molecular weights. Caprolactone was stable to 250°C, which gave an adequate temperature range for network vitrification (96–99).

Phase segregation within the film prior to pore creation can be achieved by chemically bonding the porogen to the matrix (90–92, 100). For example, chemical bonding of the norbornene porogen to the MSQ matrix was accomplished by use of triethoxy silyl groups on the norbornene.

Highly porous glassy films with air composing up to 95% of the film can be achieved through sol-gel routes. However, it does become increasingly difficult to maintain adequate network stability with closed pores at high porosity. Xerogels and aerogels are created by removing pore fluid from wet gels without pore collapse. Aerogels can be dried by numerous techniques including supercritical drying. Freeze-drying and ambient temperature drying methods can also be used (101). In one case, xerogels were formed from silica sols using a two-step acid-base procedure (102). A 70% porous xerogel with a dielectric constant of 2.2 was fully characterized in an on-chip application in 1999 (103). The pores had a diameter of approximately 6.9 nm; however, many issues relating to purity, film quality, process complexity, on-chip integration, and cost had to be addressed (104).

Many promising and useful porous materials are available for lowering the dielectric constant of a low-*k* material to the range of 2.2 to 2.5. However, dielectric constant values below 2.0 to 2.2 pose enormous challenges for any porous material. In particular, it is difficult to achieve high porosity (e.g., >50%) while maintaining adequate network mechanical properties and a

closed-pore configuration. Ultimately, the contribution of the network becomes less important to the mechanical stability of the structure when the porosity exceeds 50% to 70%. In fact, the surface area of a high-porosity nanoporous material becomes exceedingly large, which can magnify any moisture absorption or other surface-related problem.

Air Isolation

The ultimate solution for low-*k* dielectrics is simply to remove the network altogether, which greatly lowers the surface area of the dielectric because there are no pores. The resulting air cavity requires high mechanical strength from the surrounding superstructure. Several methods have been developed for fabricating on-chip and within-substrate air gaps using temporary placeholders and/or selective deposition.

In one example, an additional lithography step was used to etch holes in SiCOH between copper lines (105, 106). After the etch step, deposition of SiCOH was performed to deposit more material on the surface of the structure but not in the trench; this process pinches off the top portion of the dielectric layer. Thus, air cavities were trapped between the copper lines during the nonconformal CVD deposition of the interlevel dielectric.

Air cavities can also be formed by removing sacrificial material by wet etching (107). A SiC capping layer was used to protect the surface of the IC. Holes were etched in the SiC to provide a pathway for the etchant to remove unwanted dielectric material, leaving an air cavity. The hydrofluoric acid etchant removed a sacrificial layer (SiO_2 in this case) between the copper lines. SiLK was used on top of the sacrificial SiO_2 layer to leave a sound superstructure to continue the buildup process.

In addition, an intralevel air gap has been fabricated using a sacrificial material. Carbon was deposited as the sacrificial placeholder followed by high-temperature oxidation via air permeating through an overcoat dielectric (108). The use of a decomposable polymer avoids the potentially harmful corrosion effects of oxygen on the structure at high temperature. Furthermore, polynorbornene can be used as the sacrificial polymer for creating air gaps between copper lines, as shown in **Figure 10** (109, 110). A similar approach was used to introduce air isolation on package substrates and PWBs (111). A polymer with a lower decomposition temperature was used on the epoxy-based board so as not to cause degradation of the substrate. It was shown that the attenuation per length significantly decreased with air isolation, and the effective dielectric constant of the transmission line was 1.5.

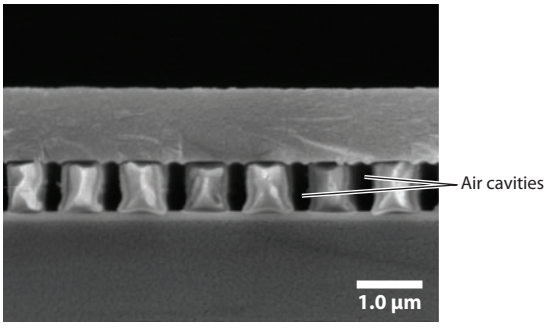


Figure 10

Air cavities created in a copper interconnect using a sacrificial polymer.

Each of the air gap–forming processes has cost and integration concerns, including that the new process steps involve new materials and process conditions. Additionally, significant reliability concerns including mechanical integrity, corrosion, and lifetime remain to be evaluated.

CONCLUSIONS

The future advancement in speed and performance of ICs is critically dependent on improvements in dielectric materials. The high data rate for future electronic systems requires that the dielectric constant (both permittivity and loss) be reduced to levels not possible today. Reduction in the permittivity is required for on-chip and short, off-chip wires. The dielectric loss is becoming increasingly important because the aggregate bandwidth for chip-to-chip communications depends on low-loss pathways. The interconnect, like all electronic functions, has entered into a power-limited regime. That is, signals must be transmitted at ever lower voltage to conserve energy. This places even greater demands on the quality of interconnect pathways and increases the need to reduce the capacitive charging of wires.

Advancements in dielectric materials have not kept up with needs and expectations because of the difficulty in producing and integrating advanced materials. The required drop in dielectric constant for chips and packages does not appear achievable with materials manufactured today. Polymeric materials offer many advantages, but their mechanical properties are so dissimilar to those of silicon and copper that their use is constrained. The lack of obvious answers may cause further delays in the scheduled implementation of low-*k* solutions. In the long term, only air (or another gas) by itself or as part of highly porous composites can meet ultralow dielectric constant needs. The integration of revolutionary dielectrics, such as polymers or highly porous insulators, has been most difficult. In sum, many challenges exist in discovering, manufacturing, and integrating next-generation dielectric solutions.

DISCLOSURE STATEMENT

The author is not aware of any affiliations, memberships, funding, or financial holdings that might be perceived as affecting the objectivity of this review.

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